REMARKS/ARGUMENTS

This Amendment is submitted in response to the Office Action dated September 6, 2006, and within the period for reply extending to December 6, 2006. The current status of the claims is summarized below.

Claims 1 and 12 are currently amended.

Claims 1-24 are pending following entry of this Amendment.

Rejections under 35 U.S.C. 102

Claims 1-24 were rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. ("Wang" hereafter) (U.S. Patent Application Publication No. 2004/0268181 A1). These rejections are traversed.

The apparatus of claim 1 has been amended to recite a boundary scan cell defined by an asynchronous flip-flop. The asynchronous flip-flop of amended claim 1 is recited as having a data input connected to receive a data signal from the device (upon which the boundary scan test is to be performed) during normal operation of the device. The asynchronous flip-flop of amended claim 1 is also recited as having a data output connected to an input/output pin of the device (upon which the boundary scan test is to be performed). Additionally, the asynchronous flip-flop of amended claim 1 is recited as having a system clock input connected to receive a system clock signal from the device (upon which the boundary scan test is to be performed) during normal operation of the device. Also, the asynchronous flip-flop of amended claim 1 recites a set input and a reset input.

Wang's teachings with regard to an asynchronous flip-flop are limited to those associated with the global scan enable generator 801 (Figure 8 and paragraph [0088]). Specifically, Wang teaches that the global scan enable generator 801 includes one

asynchronous D flip-flop 802 having a set pin and a reset pin. The global scan enable generator 801 of Wang is defined to generate a global scan enable (GSE) signal 805 at the output of the asynchronous D flip-flop 802 [0088]. Wang [0078-0079] teaches that the GSE signal 805 is provided to a unified test controller 603.

In contrast to the asynchronous flip-flop of amended claim 1, the asynchronous D flip-flop 802 of Wang does not define a boundary scan cell. Rather, according to Wang [0083], the global scan enable signal can be provided externally from automated test equipment (ATE) or generated internally by a test access port (TAP) controller. Thus, the global scan enable generator 801 and asynchronous D flip-flop 802 defined therein must exist in either the ATE or the TAP controller. It should be understood that neither the ATE nor the TAP controller defines a boundary scan cell. Therefore, the global scan enable generator 801 and asynchronous D flip-flop 802 defined therein, as disclosed by Wang, does not define a boundary scan cell as required by amended claim 1.

Amended claim 1 also requires the data input of the asynchronous flip-flop to be connected to receive a data signal from the device during normal operation of the device. In contrast to amended claim 1, Wang (Figure 8) shows the data input of the asynchronous D flip-flop 802 as having a fixed connection to a ground reference. Therefore, the asynchronous D flip-flop 802 of Wang does not teach the asynchronous flip-flop having a data input connected to receive a data signal from the device during normal operation of the device, as recited in amended claim 1.

Amended claim 1 also requires the data output of the asynchronous flip-flop to be connected to an input/output pin of the device. In contrast to amended claim 1, Wang [0078-0079] teaches that the data output of the asynchronous D flip-flop 802 is connected to provide the GSE signal 805 to the unified test controller 603. Therefore, the

asynchronous D flip-flop 802 of Wang does not teach the asynchronous flip-flop having a data output connected to an input/output pin of the device, as recited in amended claim 1.

Amended claim 1 also requires the system clock input to be connected to receive a system clock signal from the device during normal operation of the device. In contrast to amended claim 1, Wang (Figure 8) shows the system clock of the asynchronous D flip-flop 802 as having a fixed connection to a ground reference. Therefore, the asynchronous D flip-flop 802 of Wang does not teach the asynchronous flip-flop having a system clock input connected to receive a system clock signal from the device during normal operation of the device, as recited in amended claim 1.

For a claim to be anticipated under 35 U.S.C. 102, each and every feature of the claim must be taught by a single prior art reference. In view of the foregoing, the Applicant submits that Wang fails to teach each and every feature of amended claim 1 as required for anticipation under 35 U.S.C. 102. Therefore, the Office is requested to withdraw the rejection of claim 1 under 35 U.S.C. 102.

With regard to dependent claim 10, the Office has asserted that Wang teaches connection of the test data in (TDI) pin of a test access port (TAP) controller (compliant with the IEEE 1149.1 standard) to the set input of the asynchronous flip-flop that defines the boundary scan cell. Notwithstanding the fact that the asynchronous D flip-flop 802 of Wang does not define a boundary scan cell, Wang (Figure 8) teaches that the Shift_DR pin of the TAP controller is connected to the set pin of the asynchronous D flip-flop 802. The Shift_DR pin and TDI pin of the TAP controller are not the same. Therefore, Wang does not teach connection of the TDI pin of the TAP controller to the set input of the asynchronous flip-flop that defines the boundary scan cell, as recited in claim 10.

With regard to dependent claim 11, the Office has asserted that Wang teaches connection of the test reset (TRST) pin of a test access port (TAP) controller (compliant

with the IEEE 1149.1 standard) to the reset input of the asynchronous flip-flop that defines the boundary scan cell. Notwithstanding the fact that the asynchronous D flip-flop 802 of Wang does not define a boundary scan cell, Wang (Figure 8) teaches that the Update_DR pin of the TAP controller is connected to the reset pin of the asynchronous D flip-flop 802. The Update_DR pin and TRST pin of the TAP controller are not the same. Therefore, Wang does not teach connection of the TRST pin of the TAP controller to the reset input of the asynchronous flip-flop that defines the boundary scan cell, as recited in claim 11.

For a claim to be anticipated under 35 U.S.C. 102, each and every feature of the claim must be taught by a single prior art reference. In view of the foregoing, the Applicant submits that Wang fails to teach each and every feature of dependent claims 10 and 11, respectively, as required for anticipation under 35 U.S.C. 102. Therefore, the Office is requested to withdraw the rejections of claims 10 and 11 under 35 U.S.C. 102.

Because a dependent claim incorporates each and every feature of its independent claim, the dependent claim is patentable for at least the same reasons as its independent claim. Therefore, the Applicant submits that each of dependent claims 2-11 is patentable for at least the same reasons as claim 1. The Office is requested to withdraw the rejections of dependent claims 2-11 under 35 U.S.C. 102.

The Office has rejected claim 12 on the same bases as claim 1. Claim 12 has been amended to recite the same features of the asynchronous flip-flop as recited in amended claim 1. Therefore, the Applicant's arguments with respect to amended claim 1 are equally applicable to amended claim 12. Thus, the Applicant submits that amended claim 12 is not anticipated by Wang under 35 U.S.C. 102 for at least the same reasons provided for amended claim 1. Therefore, the Office is requested to withdraw the rejection of claim 12 under 35 U.S.C. 102. Additionally, the Applicant submits that each of dependent

claims 13-14 is patentable for at least the same reasons as claim 12. The Office is requested to withdraw the rejections of dependent claims 13-14 under 35 U.S.C. 102.

Claim 15 recites that the data output port of the asynchronous flip-flop is connected to a pin of the boundary scan compatible device. In contrast to claim 15, Wang [0078-0079] teaches that the data output of the asynchronous D flip-flop 802 is connected to provide the GSE signal 805 to the unified test controller 603. Therefore, the asynchronous D flip-flop 802 of Wang does not teach the asynchronous flip-flop having a data output connected to a pin of a boundary scan compatible device, as recited in claim 15.

With regard to claim 16, Wang is silent with regard to interposing a driver between the data output port (of the asynchronous flip-flop) and the pin (of the boundary scan compatible device). Additionally, Wang is silent with regard to the data output port (of the asynchronous flip-flop) being connected to an input of the driver and the pin (of the boundary scan compatible device) being connected to an output of the driver. Furthermore, the Office has not referenced any teaching within Wang of the features recited in claim 16.

Claim 17 recites that the system clock input of the asynchronous flip-flop is connected to a system clock circuit. In contrast to claim 17, Wang (Figure 8) shows the system clock of the asynchronous D flip-flop 802 as having a fixed connection to a ground reference. Therefore, the asynchronous D flip-flop 802 of Wang does not teach the asynchronous flip-flop having a system clock input connected to a system clock circuit, as recited in claim 17.

For a claim to be anticipated under 35 U.S.C. 102, each and every feature of the claim must be taught by a single prior art reference. In view of the foregoing, the Applicant submits that Wang fails to teach each and every feature of claims 15-17,

respectively, as required for anticipation under 35 U.S.C. 102. Therefore, the Office is requested to withdraw the rejections of claims 15-17 under 35 U.S.C. 102.

With regard to claims 18, Wang does not teach that a high state of the first signal causes the asynchronous flip-flop to maintain a high state. Wang also does not teach that a high state of the second signal causes the asynchronous flip-flop to maintain a low state. Furthermore, Wang does not teach that a low state of both the first signal and the second signal causes the asynchronous flip-flop to operate in a normal function mode. The Office has not referenced any teaching within Wang of the above-mentioned features recited in claim 18.

For a claim to be anticipated under 35 U.S.C. 102, each and every feature of the claim must be taught by a single prior art reference. In view of the foregoing, the Applicant submits that Wang fails to teach each and every feature of claim 18, as required for anticipation under 35 U.S.C. 102. Therefore, the Office is requested to withdraw the rejection of claims 18 under 35 U.S.C. 102. Additionally, because a dependent claim incorporates each and every feature of its independent claim, the dependent claim is patentable for at least the same reasons as its independent claim. Therefore, the Applicant submits that each of dependent claims 19-24 is patentable for at least the same reasons as claim 18. The Office is requested to withdraw the rejections of dependent claims 19-24 under 35 U.S.C. 102.

Rejections under 35 U.S.C. 103

Claims 1, 12, 15, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (U.S. Patent No. 5,574,731). These rejections are traversed.

With regard to claims 1 and 12, Qureshi does not teach a boundary scan cell defined by an asynchronous flip-flop having a set input and a reset input. Also, Qureshi

does not teach a test controller having a test clock input, a first test data output, and a second test data output. Qureshi also does not teach that a first test data output of a test controller is connected to a set input of the asynchronous flip-flop. Qureshi also does not teach that a second test data output of a test controller is connected to a reset input of the asynchronous flip-flop. Qureshi also does not teach that a test controller is configured to control the asynchronous flip-flop through a set input and a reset input.

With regard to claim 15, Qureshi does not teach at least the following features:

- connecting a first output port of a test controller to a set input port of the asynchronous flip-flop; and
- connecting a second output port of the test controller to a reset input port of the asynchronous flip-flop,
- wherein the first output port and the second output port of the test controller are connected to the asynchronous flip-flop without connecting to multiplexing circuitry intervening between the test controller and the asynchronous flip-flop.

With regard to claim 18, Qureshi does not teach at least the following features:

- communicating a first signal and a second signal from a test controller to an asynchronous flip-flop in accordance with a boundary scan timing signal, wherein the communicating is performed without having to communicate through a multiplexing circuit;
- receiving the first signal at a set input of the asynchronous flip-flop; and
- receiving the second signal at a reset input of the asynchronous flip-flop,
- wherein a high state of the first signal causes the asynchronous flip-flop to maintain a high state, a high state of the second signal causes the asynchronous flip-flop to maintain a low state, and a low state of both the

first signal and the second signal causes the asynchronous flip-flop to operate in a normal function mode.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Because Qureshi is the only reference cited in the rejections under 35 U.S.C. 103, Qureshi must teach or suggest each and every feature of the claim to render the claim prima facie obvious. As discussed above, Qureshi does not teach each and every feature of claims 1, 12, 15, and 18, respectively. Therefore, the Applicant submits that each of claims 1, 12, 15, and 18 is not rendered prima facie obvious under 35 U.S.C. 103 by Qureshi. Therefore, the Office is requested to withdraw the rejections of claim 1, 12, 15, and 18 under 35 U.S.C. 103.

Additionally, the Office has asserted that the apparatus of Qureshi teaches the apparatus of claims 1 and 12 and the method of claims 15 and 18, in that the apparatus of Qureshi performs the same function with an added multiplexer. The applicants respectfully disagree with this assertion by the Office. There is no indication in Qureshi that the apparatus of Qureshi is the same as that recited in claims 1 and 12, respectively. Also, the apparatus of Qureshi as shown in Figure 3 and referenced by the Office does not teach or suggest all the features of claims 1 and 12, respectively, as indicated above. Also, Qureshi does not teach that its apparatus functions in the same manner as recited in claims 15 and 18, respectively.

Furthermore, the Office has asserted that it would have been obvious to omit the multiplexer from the apparatus of Qureshi to arrive at the invention as recited in each of claims 1, 12, 15, and 18. Notwithstanding the fact that simply omitting the multiplexer does not make Qureshi's apparatus teach the apparatus and methods of the present invention, omission of the multiplexer in Qureshi's apparatus would render Qureshi's

apparatus inoperable for its intended purpose. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Also see MPEP 2143.01(V). Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. MPEP §2143.01 Therefore, the Applicant submits that each of claims 1, 12, 15, and 18 is not rendered prima facie obvious under 35 U.S.C. 103 by Qureshi. Again, the Office is requested to withdraw the rejections of claim 1, 12, 15, and 18 under 35 U.S.C. 103.

The Applicant submits that all of the pending claims are in condition for allowance. Therefore, a Notice of Allowance is requested. If the Examiner has any questions concerning the present Amendment, the Examiner is requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP267). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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